Electronic Version
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Claims

[c1] What is claimed is:

1. A lumped-element diplexer implemented in a multi-layered substrate comprising:

a low-pass filter circuit wherein circuit elements are disposed on a first series of layers of the multi-layered substrate and wherein a first end of the low-pass filter circuit is connected to a first port and a second end of the low-pass filter circuit is connected to a second port;

a high-pass filter circuit wherein circuit elements are disposed on a second series of layers of the multi-layered substrate and wherein a first end of the high-pass filter circuit is connected to a first port and a second end of the high-pass filter circuit is connected to a third port; and

a ground plane forming a base of the multi-layered substrate, wherein elements of the filter circuits are orientated horizontally with respect to the ground plane and are arranged in layers aligned substantially vertically, these layers being separated by a dielectric material and inter-layer connections being implemented by at least a via;

wherein an uppermost layer of the first series of layers of

the multi-layered substrate is immediately adjacent to a lowermost layer of the second series of layers of the multi-layered substrate.

[c2] 2. The lumped-element diplexer implemented in a multi-layered substrate of claim 1, wherein the elements of the high pass filter circuit are disposed on a first series of layers of the multi-layered substrate, and wherein the elements of the low-pass filter circuit are disposed on a second series of layers of the multi-layered substrate.

[c3] 3. The lumped-element diplexer implemented in a multi-layered substrate of claim 1, wherein:
the low-pass filter circuit comprises:
a first capacitor plate disposed on a first layer of the multi-layered substrate;
a second capacitor plate disposed on a second layer of the multi-layered substrate; and
a first inductor plate directly disposed on a third layer of the multi-layered substrate;
wherein the first capacitor plate is connected to the first port, the second capacitor plate is connected to a first end of the first inductor plate and the second port via a third capacitor plate of the high-pass filter circuit, and a second end of the first inductor plate is connected to the first port; and

the high-pass filter circuit comprises:
a third capacitor plate disposed on a forth layer of the multi-layered substrate;
a fourth capacitor plate disposed on a fifth layer of the multi-layered substrate;
a fifth capacitor plate disposed on a sixth layer of the multi-layered substrate; and
a second inductor plate directly disposed on a seventh layer of the multi-layered substrate;
wherein the third capacitor plate is connected to the second port, the forth capacitor plate is connected to a first end of the second inductor plate, the fifth capacitor plate is connected to the third port and a second end of the second inductor plate is connected to the ground plane.

[c4] 4. The lumped-element diplexer implemented in a multi-layered substrate of claim 1, wherein inductive elements of the filter circuits comprise plates formed as spirals.

[c5] 5. The lumped-element diplexer implemented in a multi-layered substrate of claim 1, wherein at least one inductive element of the filter circuits is formed on a plurality of layers of the multi-layered substrate.

[c6] 6. The lumped-element diplexer implemented in a multi-layered substrate of claim 1, wherein at least one

capacitive element of the filter circuits comprises a plurality of plates formed on a plurality of layers of the multi-layered substrate.

[c7] 7. The lumped-element diplexer implemented in a multi-layered substrate of claim 1, wherein the high-pass filter circuit further comprises a low frequency notch filter circuit.

[c8] 8. The lumped-element diplexer implemented in a multi-layered substrate of claim 7, wherein at least the third and fifth capacitor plates are dimensioned to have additional overlapping area in order to realize an additional capacitor equivalence.

[c9] 9. The lumped-element diplexer implemented in a multi-layered substrate of claim 1, wherein the ground forms a zeroth layer of the lumped-element diplexer.

[c10] 10. The lumped-element diplexer implemented in a multi-layered substrate of claim 1, wherein the device is realized in a multi-layered, low temperature co-fired ceramic substrate.

[c11] 11. A lumped-element diplexer implemented in a multi-layered substrate comprising:
a low-pass filter circuit comprising:
a first capacitor plate disposed on a first layer of a first

series of layers of the multi-layered substrate;
a second capacitor plate disposed on a second layer of a first series of layers of the multi-layered substrate; and
a first inductor plate directly disposed on a third layer of a first series of layers of the multi-layered substrate;
wherein the first capacitor plate is connected to a first port, the second capacitor plate is connected to a first end of the first inductor plate and to a second port via a third capacitor plate of a high-pass filter circuit of the lumped-element diplexer, and a second end of the first inductor plate is connected to the first port; and
a high-pass filter circuit comprising:
a third capacitor plate disposed on a first layer of a second series of layers of the multi-layered substrate;
a fourth capacitor plate disposed on a second layer of a second series of layers of the multi-layered substrate;
a fifth capacitor plate disposed on a third layer of a second series of layers of the multi-layered substrate; and
a second inductor plate directly disposed on a forth layer of a second series of layers of the multi-layered substrate;
wherein the third capacitor plate is connected to the second port, the forth capacitor plate is connected to a first end of the second inductor plate, the fifth capacitor plate is connected to a third port and a second end of the second inductor plate is connected to a ground plane of the

lumped-element diplexer, and wherein the high-pass filter circuit further comprises a low frequency notch filter circuit realized by additional overlapping area of the third and fifth capacitor plates.

a ground plane forming a base of the multi-layered substrate, wherein elements of the filter circuits are orientated horizontally with respect to the ground plane and are arranged in layers aligned substantially vertically, these layers being separated by a dielectric material and inter-layer connections being implemented by at least a via;

wherein an uppermost layer of the first series of layers of the multi-layered substrate is immediately adjacent to a lowermost layer of the second series of layers of the multi-layered substrate.

[c12] 12. The lumped-element diplexer implemented in a multi-layered substrate of claim 11, wherein the elements of the high pass filter circuit are disposed on a first series of layers of the multi-layered substrate, and wherein the elements of the low-pass filter circuit are disposed on a second series of layers of the multi-layered substrate.

[c13] 13. The lumped-element diplexer implemented in a multi-layered substrate of claim 11, wherein inductive elements of the filter circuits comprise plates formed as

spirals.

[c14] 14. The lumped-element diplexer implemented in a multi-layered substrate of claim 11, wherein at least one inductive element of the filter circuits is formed on a plurality of layers of the multi-layered substrate.

[c15] 15. The lumped-element diplexer implemented in a multi-layered substrate of claim 11, wherein at least one capacitive element of the filter circuits comprises a plurality of plates formed on a plurality of layers of the multi-layered substrate.

[c16] 16. The lumped-element diplexer implemented in a multi-layered substrate of claim 11, wherein the ground forms a zeroth layer of the lumped-element diplexer.